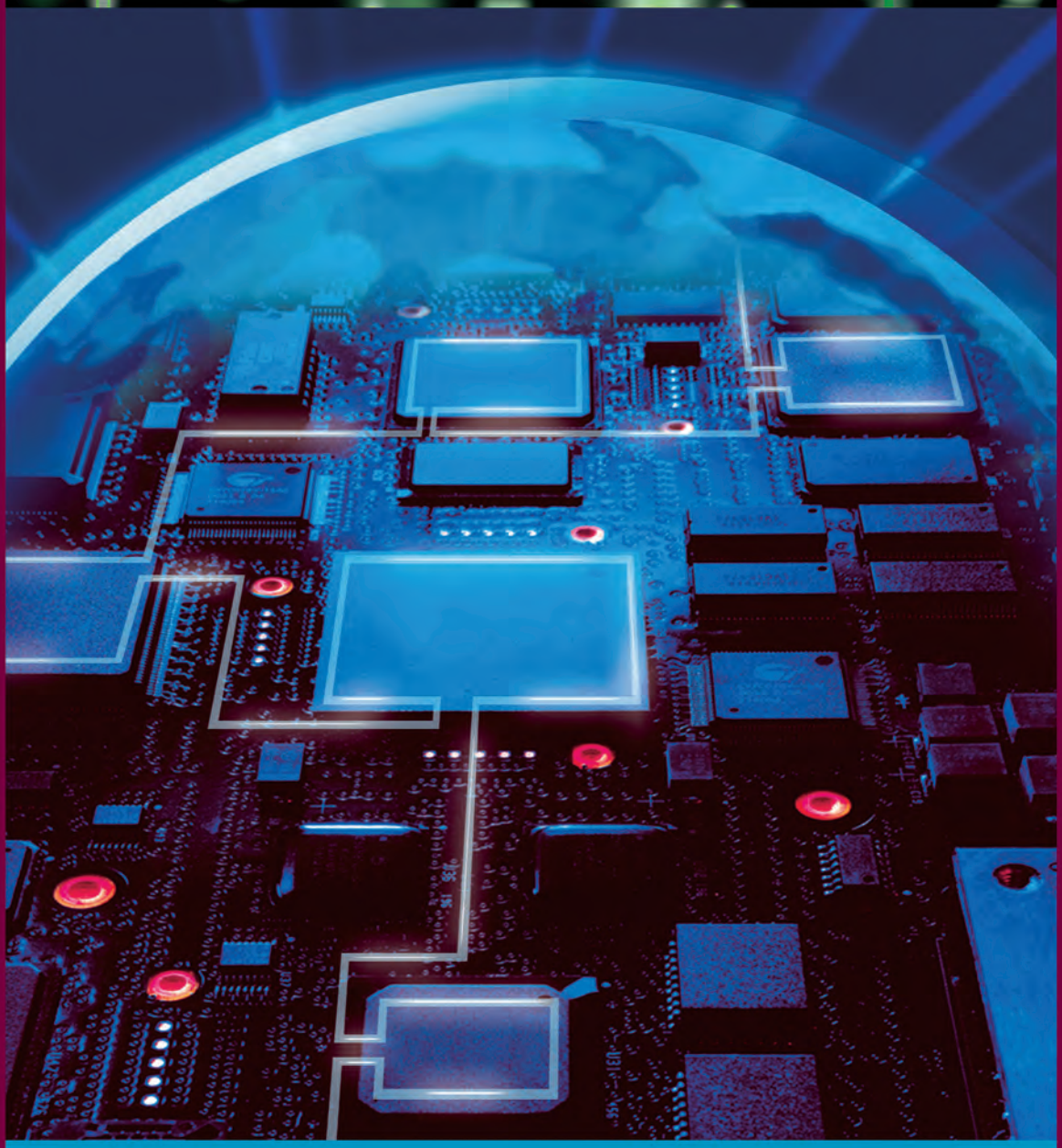
ACCULOGIC

Integrated Boundary Scan Solutions

Powered by Victory™



ACCULOGIC

- **Innovative Software**
- **Unique Patented Hardware**
- **Flexible Configuration**

ALL CONTROLLERS FEATURE:

- Adaptive Clocking™ Technology
- JPCI™ 32-bit (IEEE 1149.1, 1149.7) bus controller
- Programmable TCK rate
- Up to 32 general purpose fully programmable parallel I/O channels
- Continuous burst multi-page memory behind TDI/TDO
- Two 24 bit analog channels
- Meets addressable scan port (ASP) requirements
- Supports industry standard vector formats SVF, JAM/STAPL, IEEE 1532.
- Programmable logic levels (1.8V to 5.0V)

INTEGRATED BOUNDARY SCAN SOLUTIONS

Changes in device packaging technology (SMT), shrinking component geometries, increasing device pin-count and disappearance of test pads has challenged the practicality of conventional test in many applications. The move in most designs to operate at higher frequencies has further shortened the distances between semiconductor devices. Increased complexity and lack of physical access to circuits makes testing costly and time-consuming. Design for Test (DFT) is required to manage complexity, minimize test development time, and reduce overall manufacturing costs.

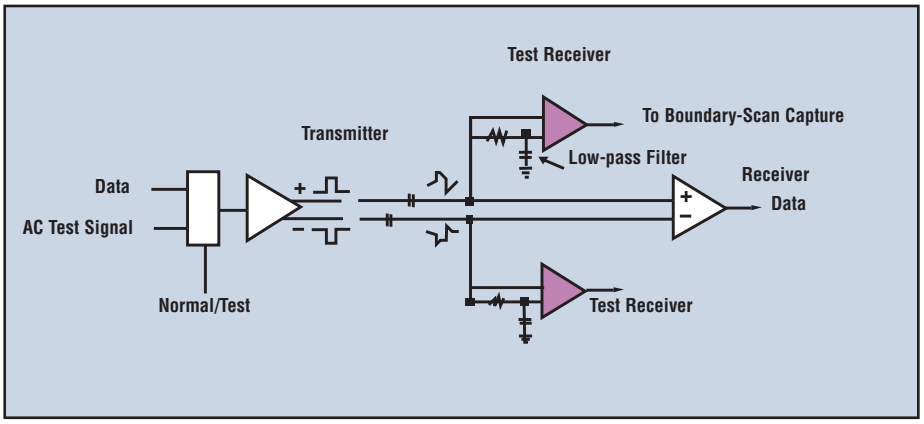
IEEE 1149.1, also known as JTAG or Boundary Scan, was introduced in 1990. This standard endeavors to solve test and diagnostic problems arising from loss of physical access caused by the increasing use of high pin count and BGA devices, multi-layer PCBs, and densely packed circuit board assemblies.

The standard outlines predefined protocols for testing and diagnosing manufacturing faults. It also provides a means for On-Board programming of non-volatile memory devices such as Flash, or In-System programming of devices like PLDs and CPLDs.

Boundary Scan Testing of Advanced Digital Networks (IEEE1149.6)

Neither IEEE Standard 1149.1-2001 nor IEEE Standard 1149.4 provide an effective and simple testing protocol with adequate fault coverage for increasingly common, newer digital networks with high-speed (1+ GBps) AC-Coupled differential serial communication interconnects. A few successful techniques have been developed for testing these applications; however, they can only be used in particular cases.

The IEEE Standard 1149.6 is an extension to IEEE Std. 1149.1-2001 that support testing of high-speed AC coupled interconnects on a PCB. This Standard is built on IEEE Standard 1149.1, using the same test access port interface of four (or five) pins, the TAP controller, and a boundary scan register.



Limited Access Testing with Boundary Scan

Acculogic offers a powerful suite of PC-based hardware and software tools specially designed for testing of electronic devices, boards and systems using the IEEE 1149.1 standard. Acculogic's comprehensive line of Boundary Scan Test tools can be effectively used in the entire product life cycle, starting with design verification and validation and continuing into pilot production and manufacturing. Use of these tools in field service and repair depots can help further to reduce test cost and cycle time.

Device Programming with Boundary Scan

Boundary Scan provides the added benefit and convenience of using the embedded resources of Micro Controllers and Processors for programming the embedded devices. In addition Boundary Scan offers On-Board Programming of Flash, E2 memory devices and In-System Programming (ISP/ISC) of CPLDs, PLDs, FPGAs. Acculogic's family of Boundary Scan controllers rely on the company's patented Adaptive Clocking™ technology to provide the fastest and most reliable means for delivering program data to the target.

BOUNDARY SCAN HARDWARE

ScanMaster™ Boundary Scan Controller family

At the heart of Acculogic's boundary scan support product line is the ScanMaster family of advanced, high speed IEEE1149.1 and IEEE 1149.6 (JTAG) controllers. Based on our proprietary bus controller JPCI™ and backed by our patented Adaptive Clocking Technology™, ScanMaster is available in a wide variety of industry standard bus architectures to support integration into any test system for use in design verification, production test, and on-board device programming applications.

- ScanMaster - PCI
- ScanMaster PXI
- ScanMaster VXI
- ScanBox LAN USB2
- ScanRack LAN USB2

Adaptive Clocking Technology™

Patented Adaptive Clocking Technology eliminates instabilities typically associated with boundary scan (JTAG) operation at high clock rates (TCK) due to path delays. Adaptive Clocking compensates for signal path delays allowing the ScanMaster controller to operate at the maximum TCK rate supported by the target device, and enables reliable testing over cable lengths of up to 15 meters (50 ft) without the use of a retiming pod.

Without Adaptive Clocking Technology, expect:

- Reduced TCK rate, longer test times
- Physical constraint of short cables (<18"), reduced configuration flexibility
- Need for signal retiming hardware in your test system or fixture

ScanBox™ for Remote Distributed Boundary Scan Testing (Internet or Intranet)

ScanBox is the next generation Boundary Scan (JTAG) test platform. Based on Acculogic's high performance JPCI 32-bit TAP controller chip with patented Adaptive Clocking Technology. ScanBox built-in Ethernet and USB2 provides the flexibility and performance required for Remote Distributed Testing (RDT). ScanBox combines built-in Boundary Scan controller and PC-standard connectivity with the modularity and size reduction of card cage-based systems. ScanBox's compact, flexible package, high-speed data rates and reliable operation meet the needs of R&D and manufacturing and test engineers delivering electronics for the aerospace/defense, automotive, industrial, and medical and consumer electronics markets.

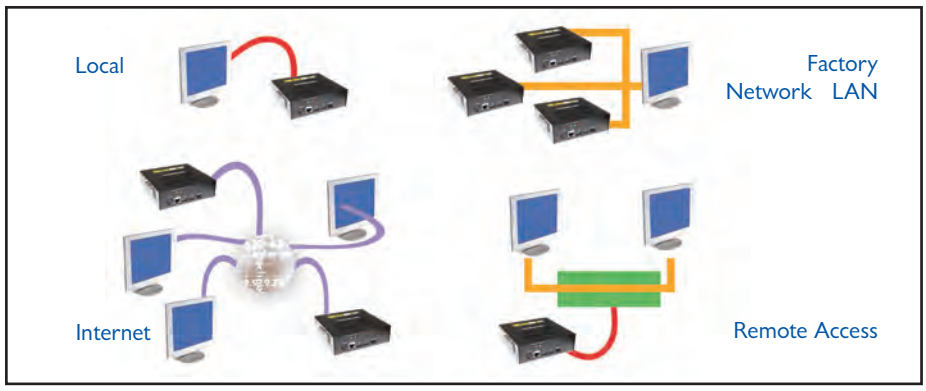
Remote access and distributed testing

Remote control and distributed testing is essential for Boundary Scan (JTAG) applications such as design validation, environmental tests, automated factory test, repair and calibration. ScanBox is based on industry standard Ethernet technology which has a wide general acceptance. Advantages of using Ethernet include TCP/IP error checking, fault detection and long inter-device connectivity. Ease of cable routing and inexpensive networking hardware. Ethernet enables the ScanBox to be deployed in a local, intranet or internet based distributed environment.

ScanRack™

ScanRack system is based on the ScanBox technology housed in an industry standard 19 inch, one U rack-mountable enclosure. ScanRack provides flexible self contained configuration to meet most demanding production requirements.

1. ScanRack SR-3 is configurable with up-to 3 independent Boundary Scan Controllers
2. ScanRack SR-1 includes one Boundary Scan controller and a ScanMultiplier with three TAP ports.



ScanMaster-PCI

ScanMaster-PXI

ScanMaster-VXI

ScanBox

ScanRack

Panther III

ScanMultiplier4 with enclosure

Peripherals

ScanMultiplier ™ with its intelligent controller routes serial data streams to and from up to 16 Boundary Scan Chains under program control. Multiple scan paths can be addressed individually or daisy chained to maximize fault coverage. ScanMultiplier can also increase test and programming throughput by providing simultaneous access to up to 16 targets for gang-programming and testing.

ParallelRiter™ offers a powerful and easy to use solution for providing parallel Input/Output (I/O) "Scan Channels" access to device under test (DUT) for on-board programming and enhancing boundary scan test coverage, including fault coverage of non-scan components. ParallelRiter operates with Acculogic ScanMaster family of boundary scan controller cards and transforms the generated serial stream to parallel data that is then applied to the target via test pads, headers, or connectors.

Key ParallelRiter features:

- 64 fully programmable, bidirectional digital I/O channels per card
- Data rates of up to 20 MHz (TCK)
- Programmable voltage levels 3.3V and 5V

Panther III Boundary Scan Station Controller

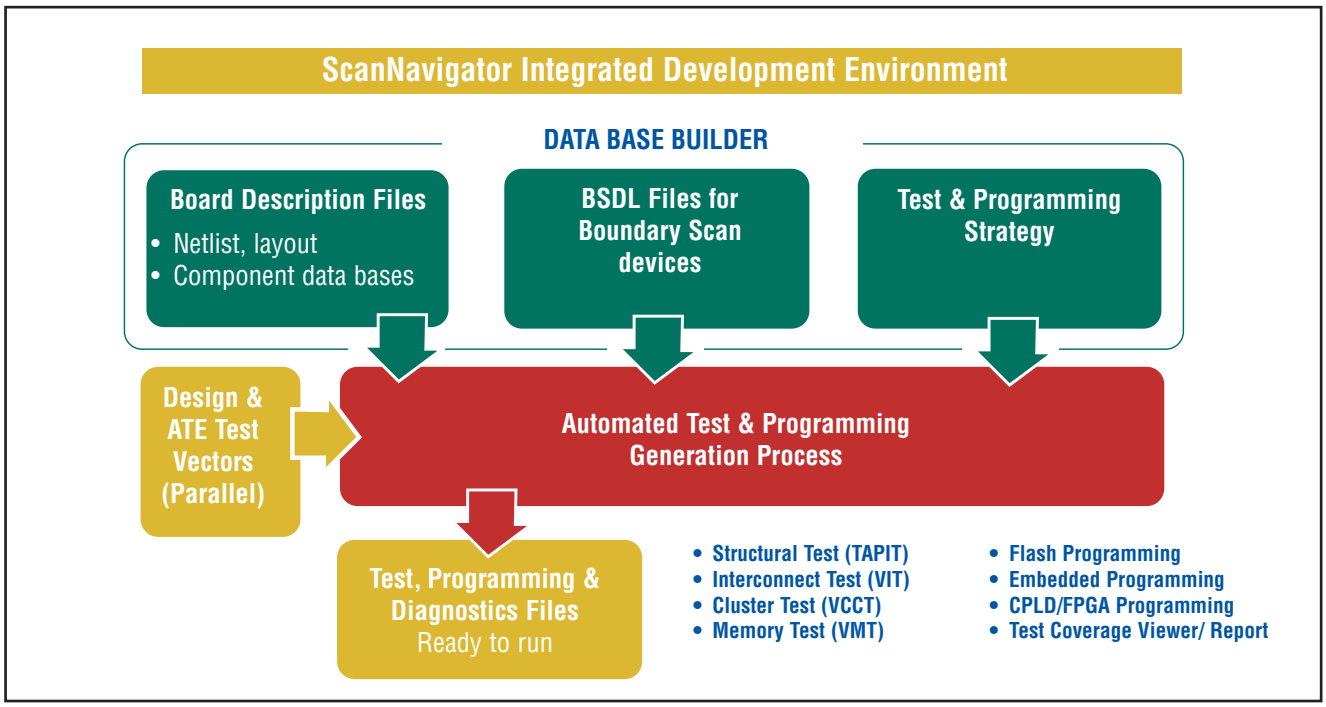
Flexible Deployment in End-user System

Acculogic boundary scan and on-board programming products easily integrate into the leading in-circuit (Acculogic Scorpion, Teradyne, GR, Agilent), and commercial and DoD functional test platforms, and are also available in packaged standalone bench top or rack mounted test systems. The Acculogic Panther III features its own PC with the ScanNavigator Integrated Development and Runtime environment, monitor, keyboard and a PCI chassis that can be configured with ScanMaster, ScanMultiplier, ParallelRiter and IEEE 488 Controller cards to meet the most demanding boundary scan test and programming applications.

Third Party Test Hardware Support (Digital Channel/IO Cards)

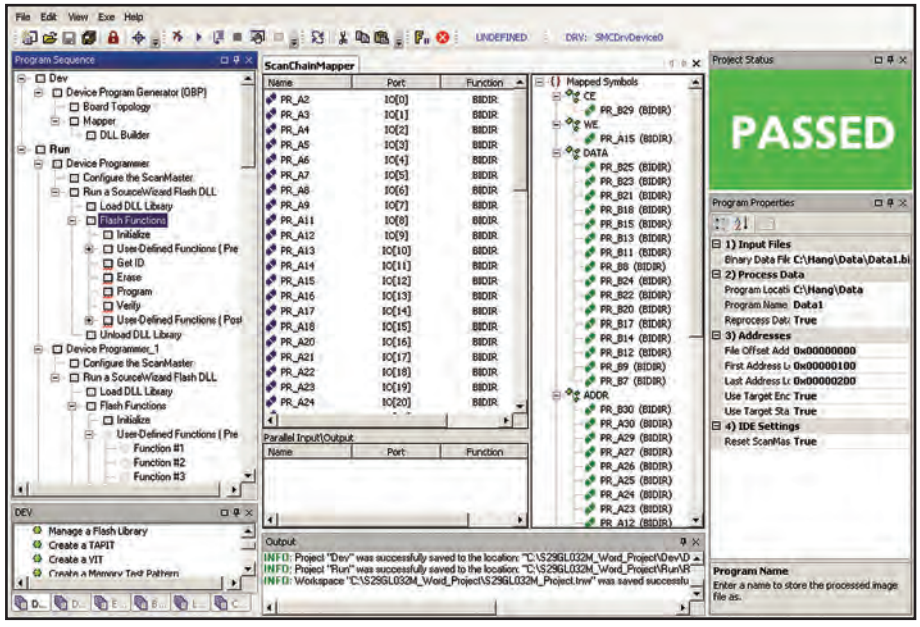
Acculogic is committed to supporting third party Digital test channel/ IO cards/peripherals for use in functional testing. Currently we offer flexible and seamless integration with many off-the shelf products from various test equipment manufacturers.

ScanNavigator™ BOUNDARY SCAN SOFTWARE

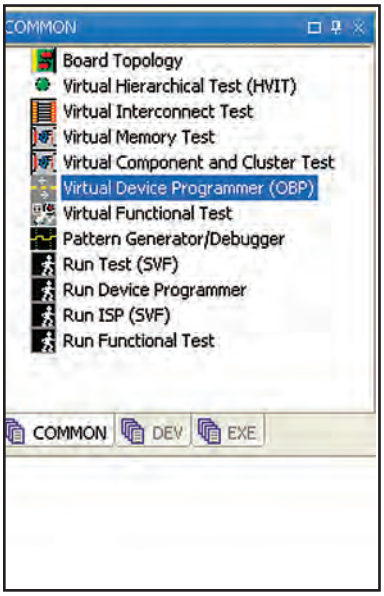


Powered by Victory™

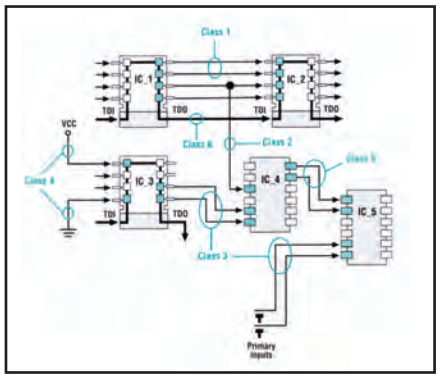
Acculogic's flagship ScanNavigator Boundary Scan Test and Programming Framework consists of test, programming, and run-time modules that utilize Microsoft's .NET technology and W3C XML to simplify test generation, increase productivity, and allow full integration of test data, programming information, and diagnostic databases with Acculogic's testability and coverage analysis tools. Based on the premise that all JTAG test and Device programming activities rely on a number of common data preparation steps, ScanNavigator architecture is optimized for data sharing and portability to reduce development time and increase data reuse.



ScanNavigator Development



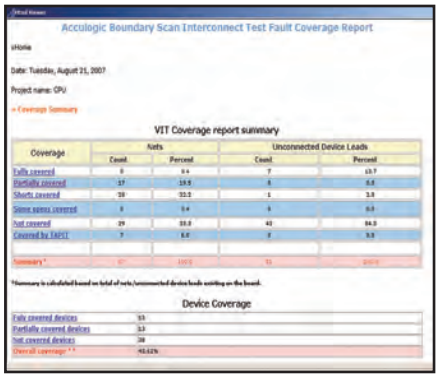
ScanNavigator Development Templates

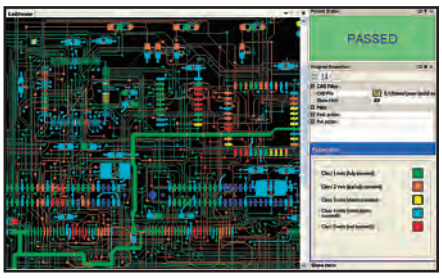


Network classes recognized by VIT:

CLASS 1 *Pure scan nets.*
CLASS 2 *Partial scan nets that have at least one scan driver, cone scan receiver, and one non-scan device lead.*
CLASS 3 *Nets where scan outputs or tester channels drive one-scan inputs.*
CLASS 4 *Boundary-scan inputs connected to power or ground.*
CLASS 5 *Non-scan nets with no tester access.*
CLASS 6 *TAP nets.*

Coverage Report





CAD Based Coverage Viewer

ScanNavigator™ Integrated Development Environment (IDE) is powered by the VICTORY boundary scan Automated Test Pattern Generation (ATPG) engine, and provides a rich set of easing to use, novice-friendly features that include data creation wizards, reusable test development and execution templates, and a powerful sequencer engine to streamline the test generation process.

ScanNavigator's modular architecture enables you to pick and choose from the following list of application-specific software modules. From DFT analysis and prototype validation to production and field test, ScanNavigator provides access to the right tools that fit your needs and your budget.

The ScanNavigator RunTime Environment (RTE) provides a broad range real-time control features to steer the flow of your boundary scan test program based on the pass/fail status of a particular test step. ScanNavigator RTE can be deployed as a standalone test executive or as a test step in a National Instruments TestStand sequence which is a common application when Acculogic JTAG products are integrated into larger test systems.

ScanNavigator's Access Analyzer Module automates pre-layout testability analysis

Access Analyzer is typically used after schematic capture and before CAD layout for assemblies that have a mix of scan and non-scan devices. Access Analyzer identifies all the pure scan nets and scan control nets (TDI/TDO interconnects) where physical test points can be eliminated without jeopardizing test coverage.

It's report also identifies nets shared by scan and non-scan components where physical access may be reduced or eliminated because enough visibility and control is provide by the scan component.

ScanNavigator's Virtual Interconnect Test Module (VIT) offers 100% pin-level fault coverage

The ScanNavigator VIT module generates patterns to test boundary-scan nets using only the virtual access provided by the Boundary Scan (JTAG) circuitry. On pure boundary-scan nets, VIT provides full fault coverage of all open and shorts faults from silicon to lead bonds, from solder bonds to the circuit board itself. VIT patterns are generated automatically from a circuit netlist and the BSDL models of boundary-scan devices.

IEEE 1149.6 Support

ScanNavigator supports IEEE1149.6 that can be incorporated into any Virtual Interconnect Test, making the implementation of 1149.6 tests practically transparent to the user. The same design description, netlist and constraint definitions that are used with both 1149.1 and 1149.6 interconnect tests. ScanNavigator automatically detects the dot6 device from the associated BSDL models, and selecting EXTEST PULSE instead of EXTEST will automatically generate the appropriate vectors.

ScanNavigator treats the coupling capacitors as transparent devices for AC testing and as an open for DC testing. The test coverage generated for both types of testing is combined in a comprehensive test coverage report.

- Testing of AC-coupled and differential nets
- Automatic detection of IEEE1149.6-compliant devices
- Integrated with IEEE 1149.1 static testing
- Support of special IEEE 1149.6 features

IEEE 1149.7 Support

ScanNavigator's Virtual Component/Cluster Test Module (VCCT) extends access to non-scan circuitry

The ScanNavigator VCCT module uses boundary scan access to detect open and stuck-at faults on the leads of non-scan devices, eliminating the need for physical access to the signal pins of those devices. VCCT can be used to test either a single component or a cluster of non-scan components.

VCCT uses the scan cells of boundary scan devices as virtual test channels to drive stimulus to and detect response from non-scan logic devices. Patterns for component and cluster test may be available from an in-circuit test library, a design pattern library, or they may have to be created.

ScanNavigator's Hierarchical VIT (HVIT) & VCCT (HVCCT) Test Modules extended pin-level fault coverage

ScanNavigator's Hierarchical VIT and VCCT modules generate test patterns and diagnostics using multiple netlists (multiple assemblies for example mother/daughter board designs) through an intuitive and graphical neltlist merging interface. Includes:
- Hierarchical netlist mapper
- Hierarchical chain definition

ScanNavigator's Virtual Memory Test Module (VMT) finds faults in internal device logic

Even though memory devices such as RAMs do not currently support IEEE1149.1, processors, ASIC's, FPGAs and other programmable parts that often control them do. The control devices for which JTAG standard is implemented can provide access to the memory device pins, therefore facilitating on-board RAM testing. The Virtual Memory Test generation module automatically creates test patterns from an address, data and control line specification template that detect faults on RAM devices.

ScanNavigator's Boundary-Scan Intelligent Diagnostics (BSID) quickly isolates faults

BSID generates clear diagnostic information for failures that occur during the execution TAPIT, VIT and VCCT tests. When a boundary-scan test fails, BSID uses the failure data captured by the tester and compares it with expected test results to isolate the failing devices and nets. To generate diagnostics for a virtual cluster test, BSID can use fault-dictionary techniques if a fault-dictionary database is supplied. BSID quickly isolates common faults such as shorts, opens, and stuck-at pins, as well as difficult-to-detect strong driver shorts and bus faults.

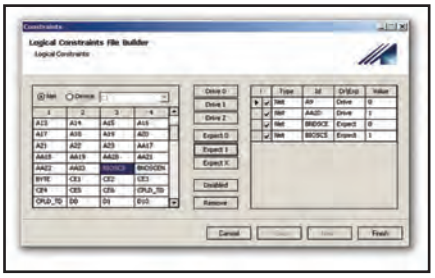
```
VIT: TEST FAILED: vit

 Fault: STUCK AT 0
   Stuck input, possible open at lead U1_22.
   Net: Name: AA22
        Device: U4  Lead: 19  scan output
        Device: U6  Lead: 7  input
   Net: Name: A22
        Device: U1  Lead: 22  scan input/output
        Device: P2  Lead: 29  analog
        Device: U3  Lead: 8  input
        Device: U5  Lead: 8  input
        Device: U6  Lead: 13  output
  Detect points: lead U1_22
```

Intelligent Diagnosis

ScanNavigator's Flash Memory and PLD Programming

For flash and other non-volatile memory devices that are accessible via boundary scan devices, ScanNavigator provides the tools and user environment to help even novice developers generate flash programming applications in just a few minutes. ScanNavigator templates organize and present scan chain-to-device pin mapping, memory data specification and delivery tasks through graphical display and builder tools. The flash library browser contains a wealth of pre-existing flash models, and provides a wizard for building your own models. For in-system programmable CPLDs and FPGAs, ScanNavigator supports programming files direct from vendor tools in SVF, JAM/STAPL and IEEE 1532 formats.



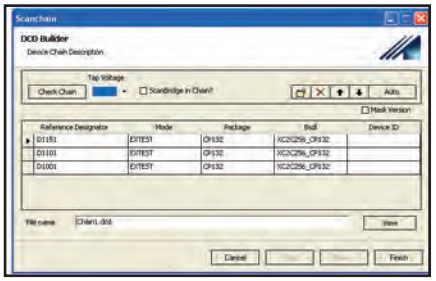
ScanNavigator Constraint Builder Wizard

Coupled with the speed and power of the ScanMaster controller, on-board programming of flash memory in the ScanNavigator environment effectively combines performance with ease of use.

ScanNavigator's Core Instrumentation Test and Programming.

For silicon embedded memories accessible directly or via core processor, ScanNavigator provides tools to automatically (in most cases) generate device programming routines in minutes. ScanNavigator templates organize and present scan chain and internal register bit mapping, memory data specification and delivery tasks through a graphical display and builder tools. The device library browser contains a large number of pre-existing programming models.

ScanNavigator's simple register access interface provides powerful means for developing complex at speed functional patterns for at speed testing.



ScanNavigator Chain Builder Wizard

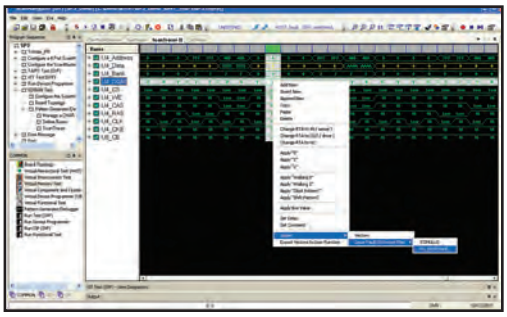
SCANTRACER™

Graphical test pattern generator for non-scan device clusters

ScanTracer™ test pattern development and debug software combines the ease of graphical programming, the speed of the ScanMaster Controller card, and the power of ScanNavigator Integrated Development Environment to get you the best possible test coverage in the shortest possible time.

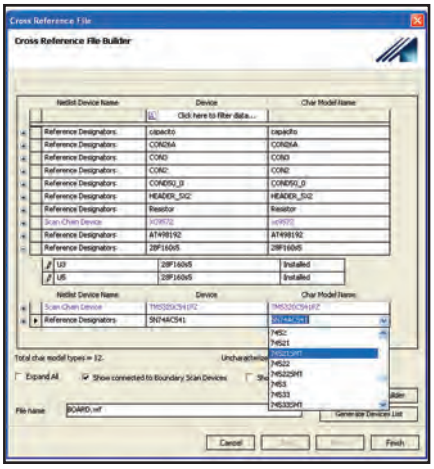
ScanTracer is ideal for generating tests of non-scan device clusters that share leads with JTAG compliant devices. You simply identify and map the signals, device leads or net names you wish to include in the test, and then start creating test patterns for the DUT (device under test). The test patterns can be defined, and later edited, at the bit level, bus level or burst level. As an efficiency feature, ScanTracer allows you to save patterns defined in a test so you can reapply them, or an edited version of them, in another test.

Additionally, ScanTracer supports import of Teradyne's LASAR and third party simulation vectors for the reuse of existing simulation and test patterns.



ScanTracer development (wareform editor)

Cluster tests generated in ScanTracer can be run from the ScanTracer GUI in burst or single step mode, or executed as part of a larger ScanNavigator sequence. Patterns where observed response data differs from expected response data are clearly displayed in the GUI to assist in test debug.



ScanNavigator Cross-reference Builder

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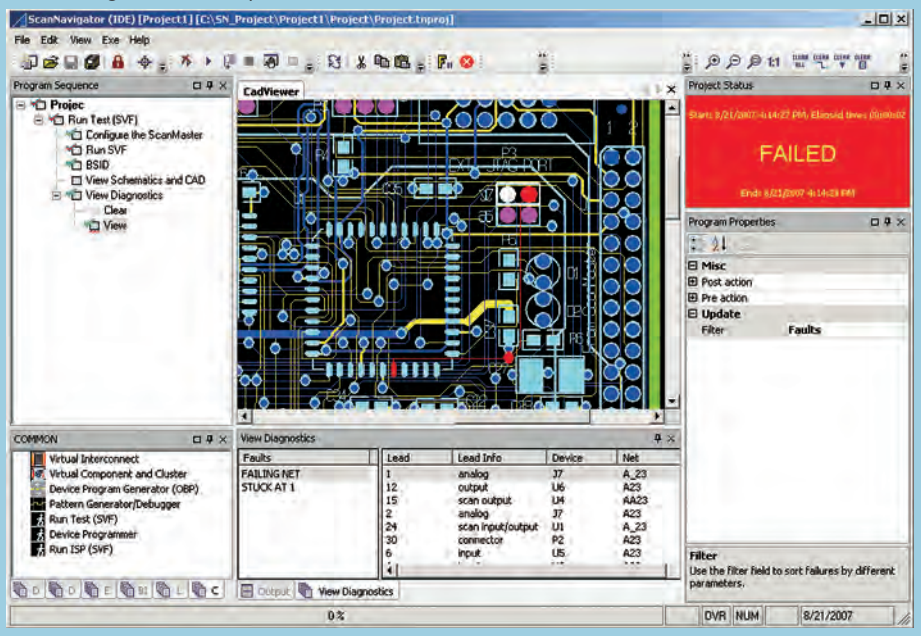
INTELLIGENT DIAGNOSTIC VIEWER

Intelligent Diagnostic Viewer for pin-point fault isolation

The Intelligent Diagnostic Viewer (IDV) is an easy to use debugging and troubleshooting production tool. The IDV works in conjunction with both the board layout and schematic viewer in order to help detect and correct board failures and defects in manufacturing. IDV, through an easy to read graphical user interface, supplies the essential information to easily pinpoint board failures, correct them and move forward in the testing and validation process.



Run time Diagnostic

Acculogic Board Test Line of Products and Services :

- Flying Scorpion - Double sided multi-probe (22) Probe System
- InCircuit Scorpion 7000 Series - Low Cost ICT/MDA System
- In-Line In-Circuit Test ILS-1000
- Tracer 2000 PXI Based Functional Test System
- XMATIC CAD processing Software
- ScanNavigator Boundary Scan Software Tools
- ScanMaster high performance Boundary Scan Hardware
- Panther III Boundary Scan Station Controller
- ScanBox/ScanRack Internet/Internet remote access Boundary Scan Controller
- In-Fixture Electronics
- Test Engineering Services including ICT programming and Fixture design
- Application Specific Functional Test System design and fabrication

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